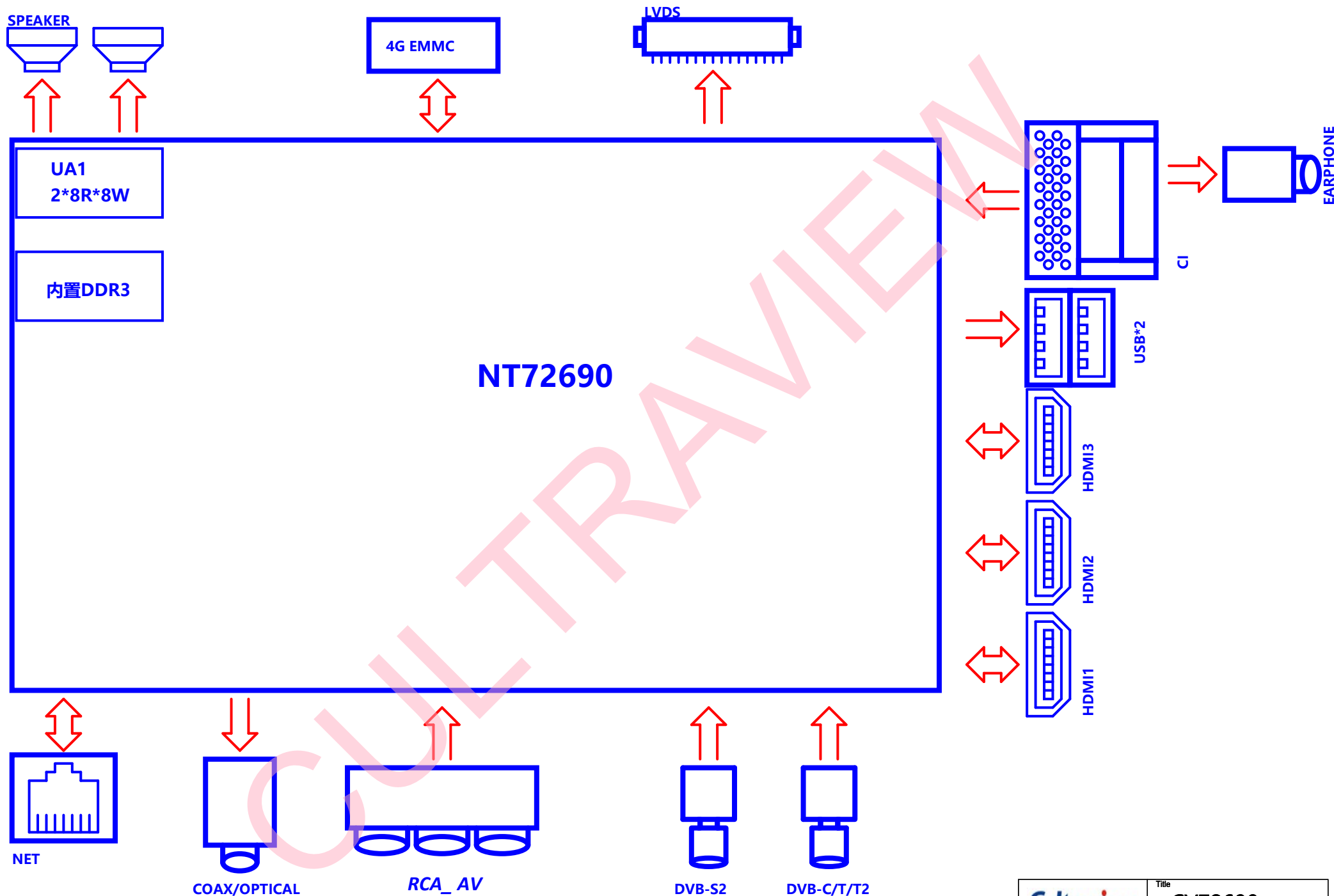
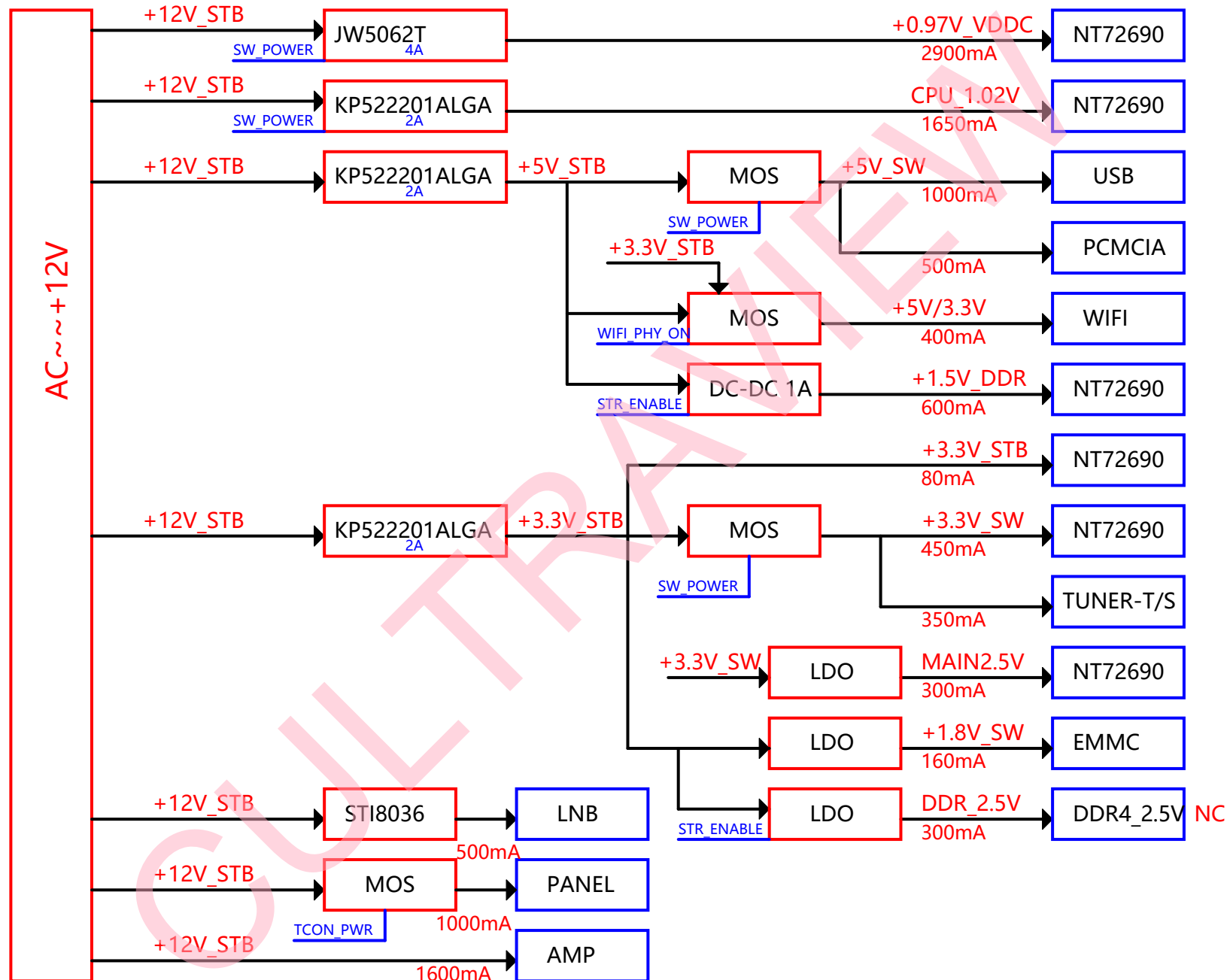
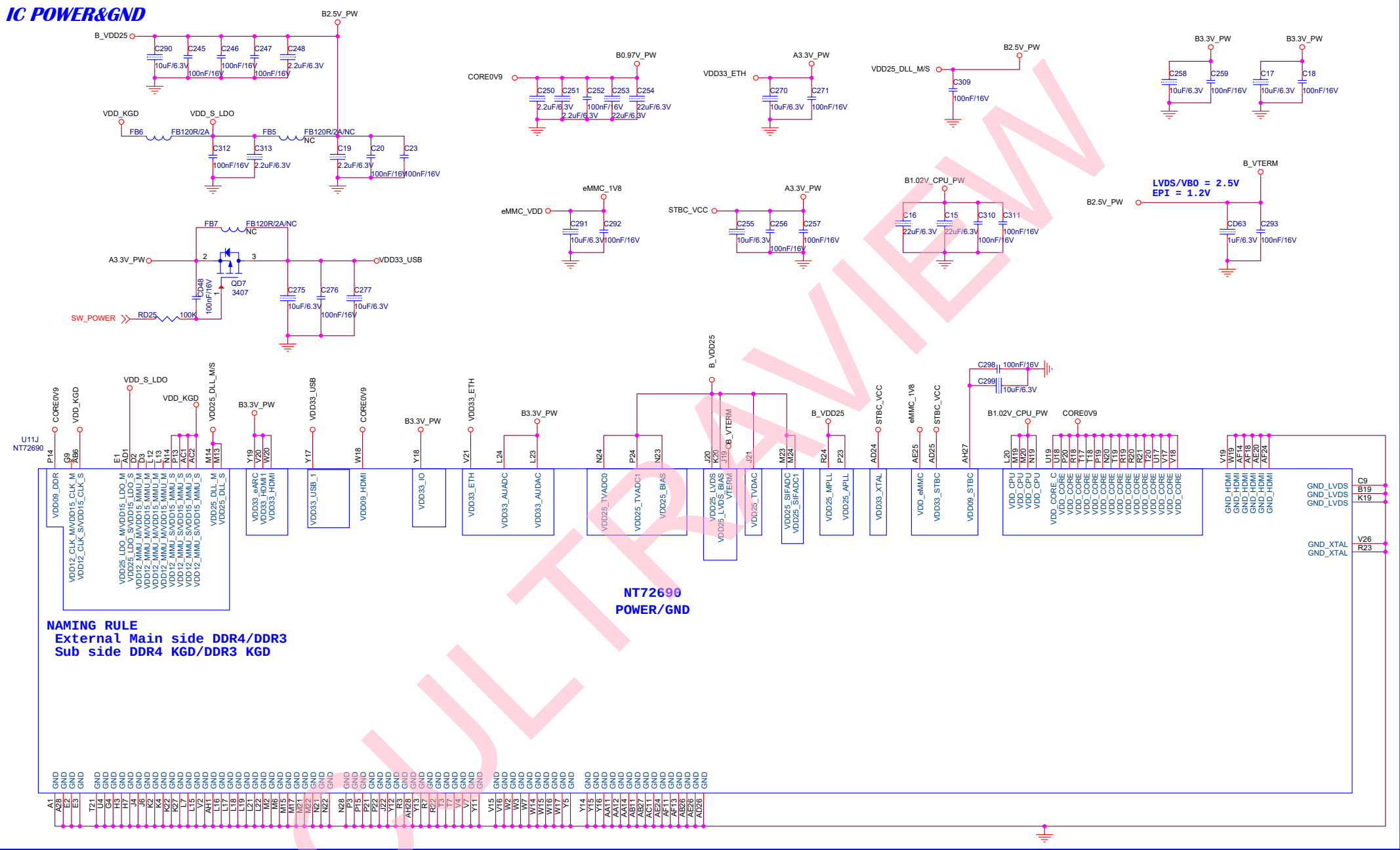




POWER SUPPLY ARCHITECTURE

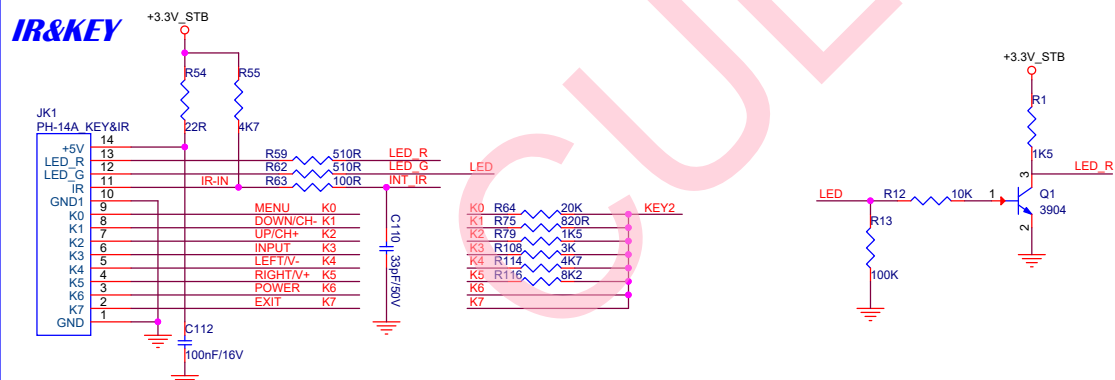
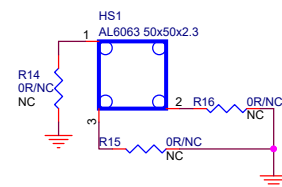


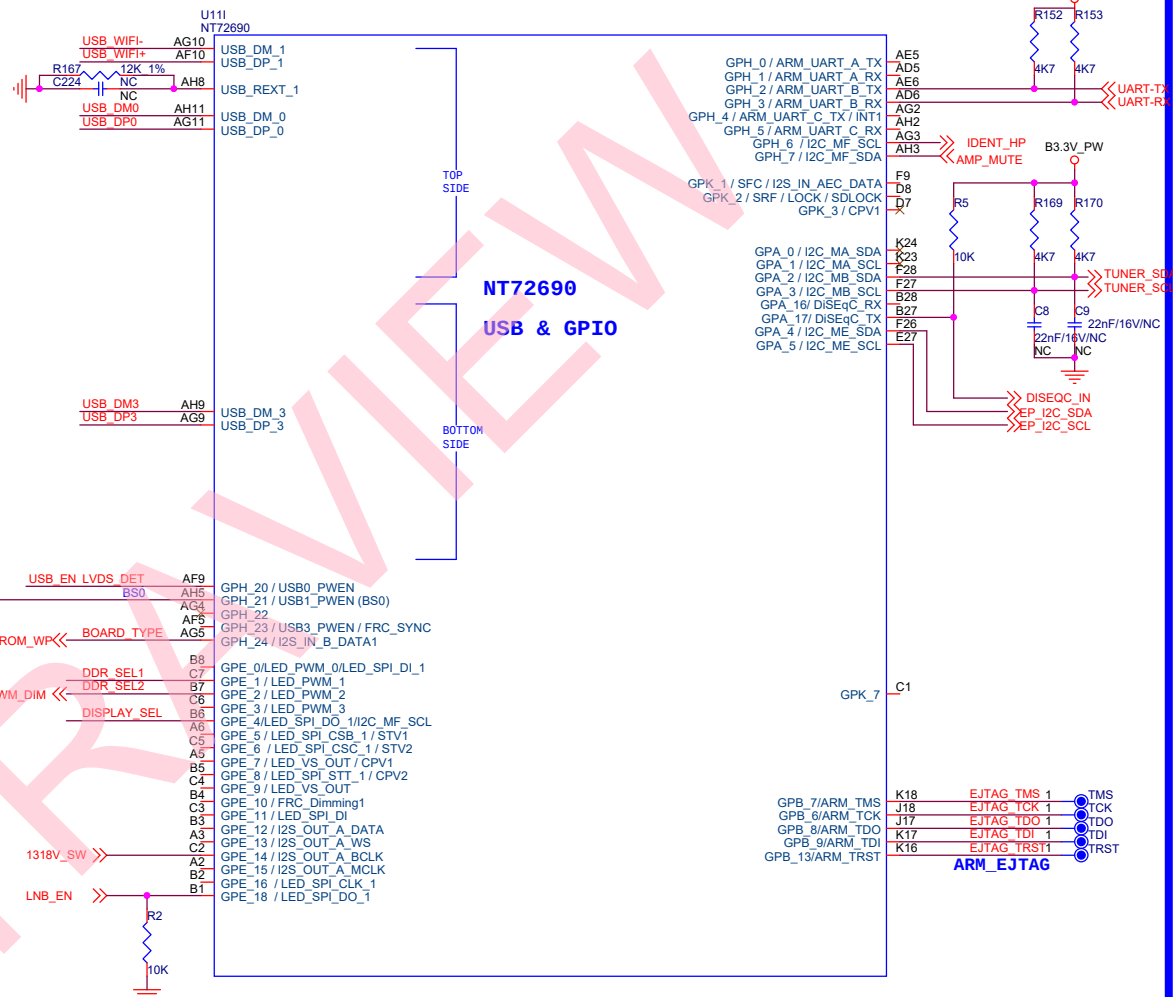
IC POWER&GND



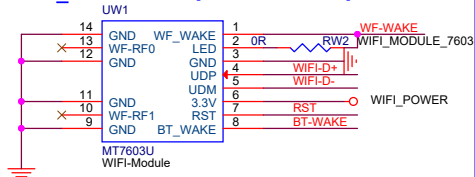
NAMING RULE
External Main side DDR4/DDR3
Sub side DDR4 KGD/DDR3 KGD

NT72690
POWER/GND

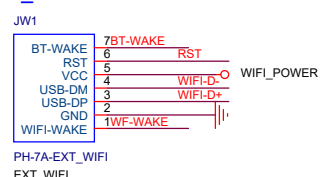




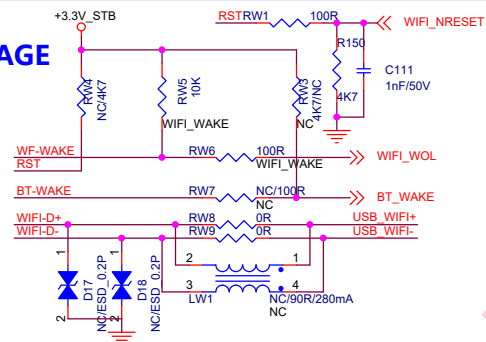
WIFI MODULE(7603/7663)



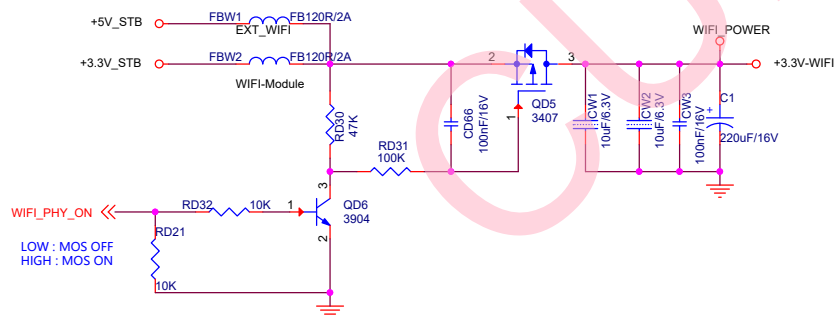
EX WIFI



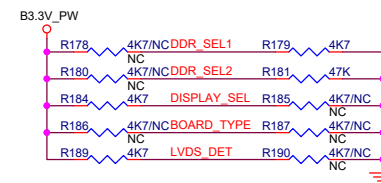
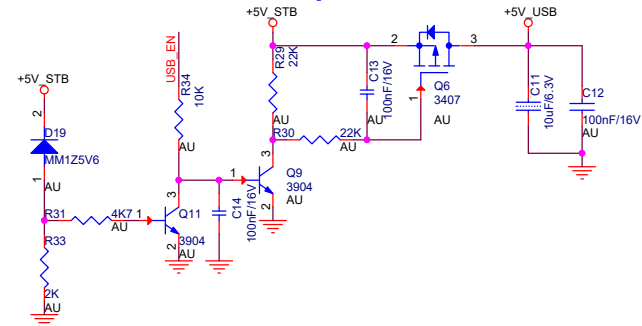
SIGNAL OFFPAGE



POWER SWITCH



Australian Certification Requirements



[illegible]

The schematic diagram illustrates the electrical connections for the UART module. It shows the UART module connected to the HDMI module through a 1Kx4 resistor network. The UART module is also connected to the UART module via a 100nF/16VIN capacitor. The UART module is connected to the UART module via a 100nF/16VIN capacitor.

HDMI1

J10

21 DATA2+
21 DATA2_SHIELD
22 DATA1+
22 DATA1_SHIELD
22 DATA0+
22 DATA0_SHIELD
23 CLK+
23 CLK_SHIELD
23 CEC
23 NC
23 SCL
23 SDA
20 CEC_GND
20 +5V POWER
20 HOT PLUG

U15 ESB-CS0806S/NC NC

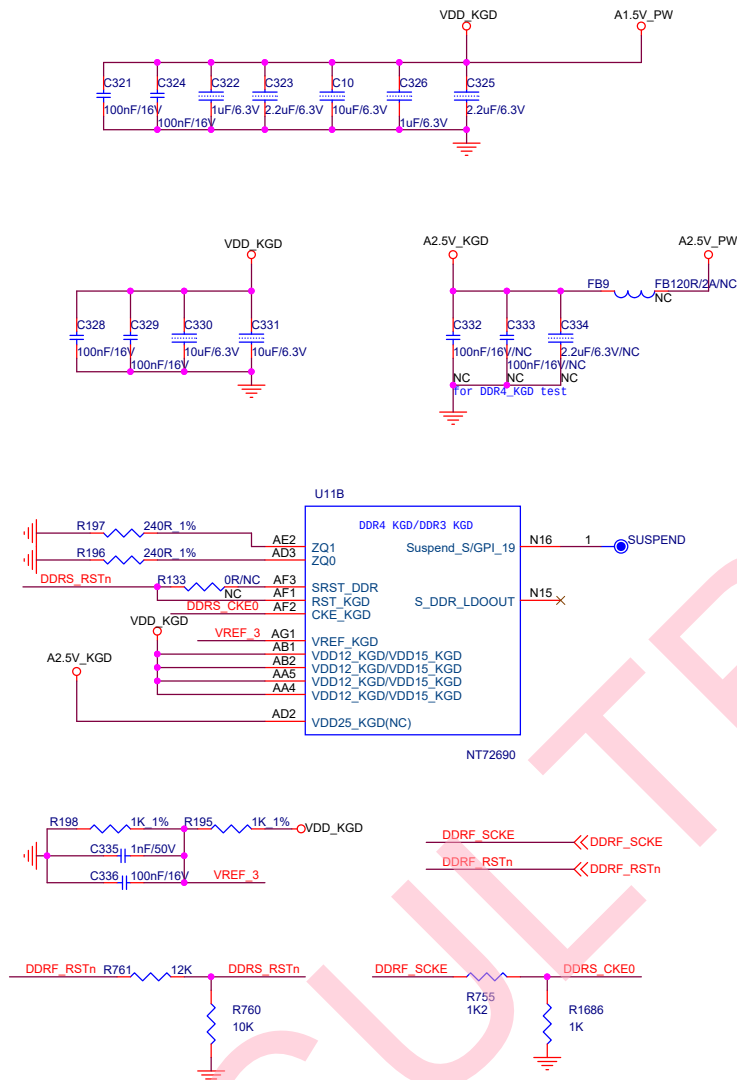
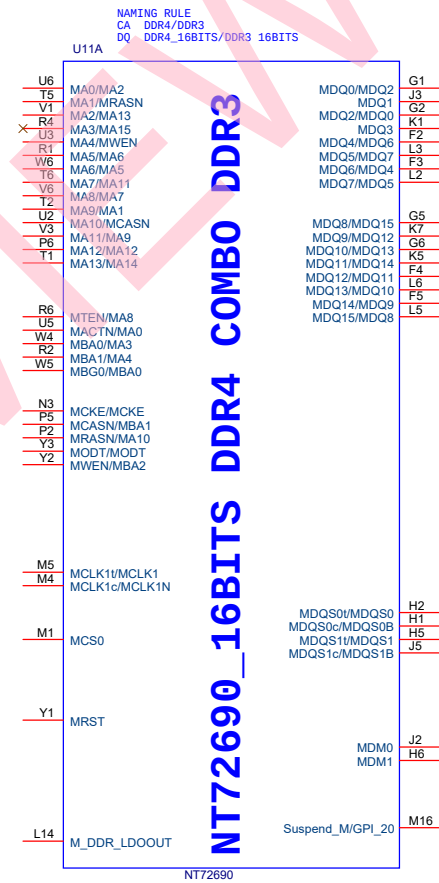
1 RXD2+
2 RXD2-
3 RXD2+
4 RXD1+
5 RXD1-
6 RXD1+
7 RXD0+
8 RXD0-
9 RXD0+
10 RXDC+
11 RXDC-
12 RXDC-
13 CEC
14 HDMI_UART_EN
15 HDMI_SCL
16 HDMI_SDA
17
18
19

U19 ESB-CS0806S/NC NC

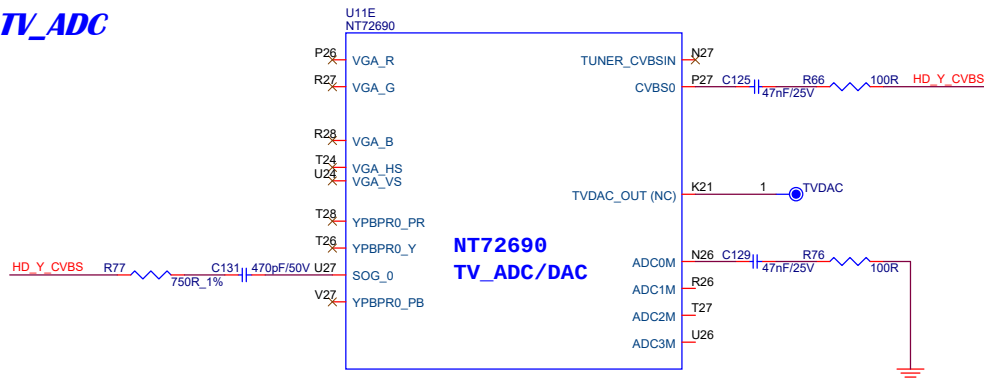
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2 RXD1+
3 RXD1+
4 RXD2-
5 RXD2+
6 RXD2+
7 RXD2+
8 RXD1-
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10 RXD1-
11 RXD1+
12 RXD1-
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377 RXD1

[illegible]

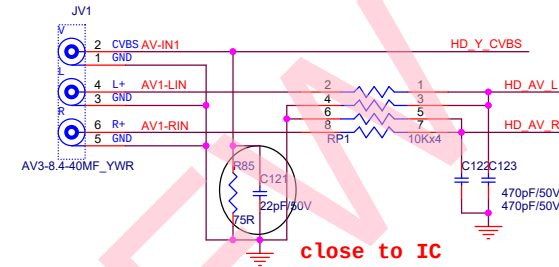
DDR_S

**DDR_M**

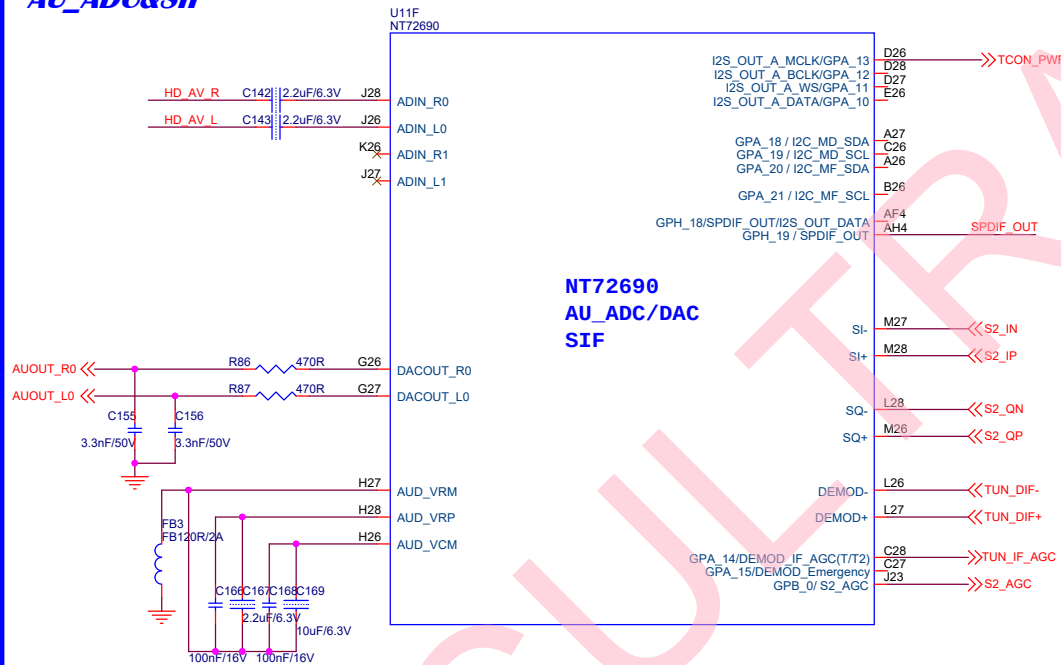
TV_ADC



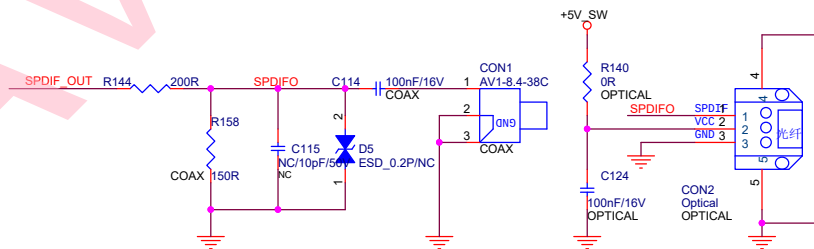
AV1_IN

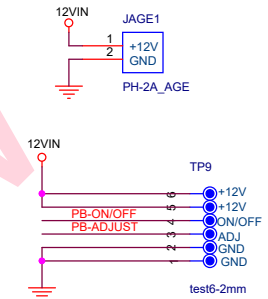
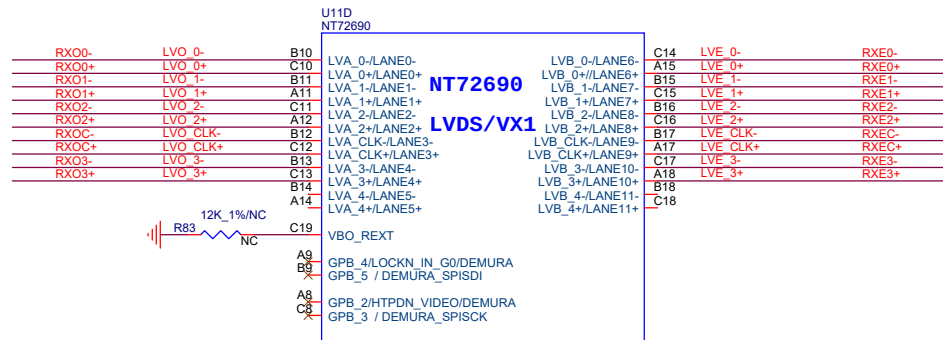


AU_ADC&SIF

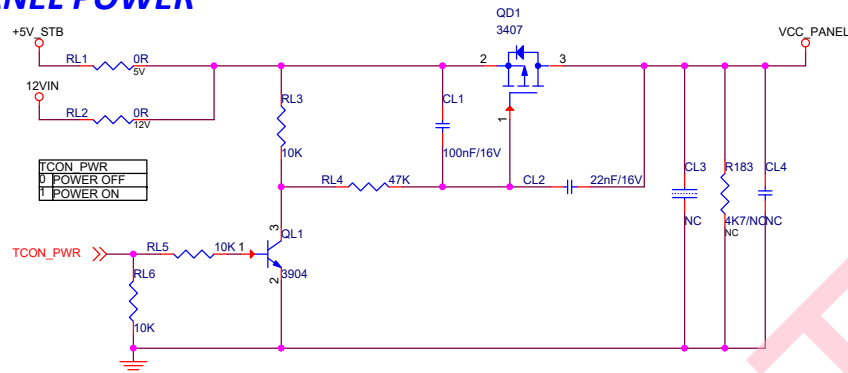


SPDIF OUT

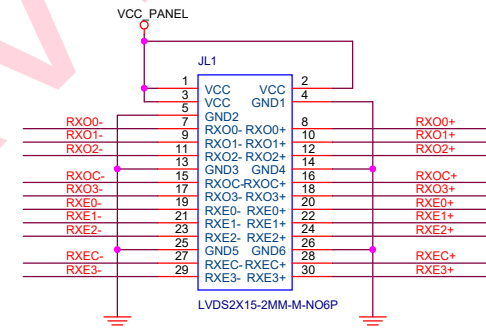




PANEL POWER



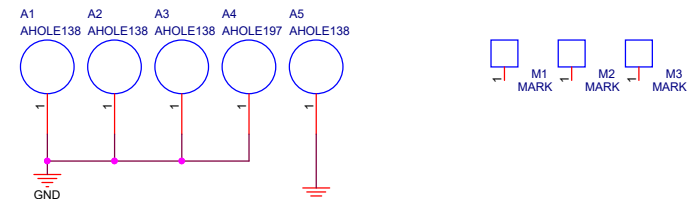
LVDS



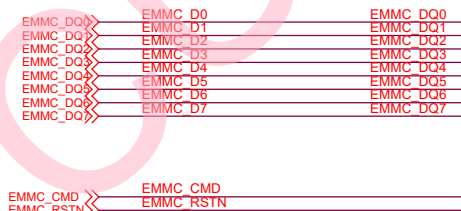
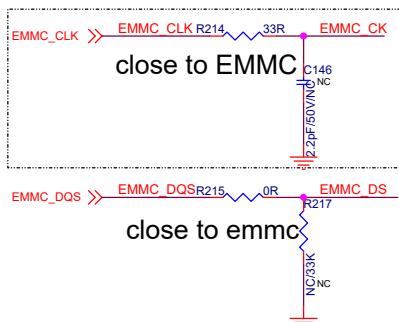
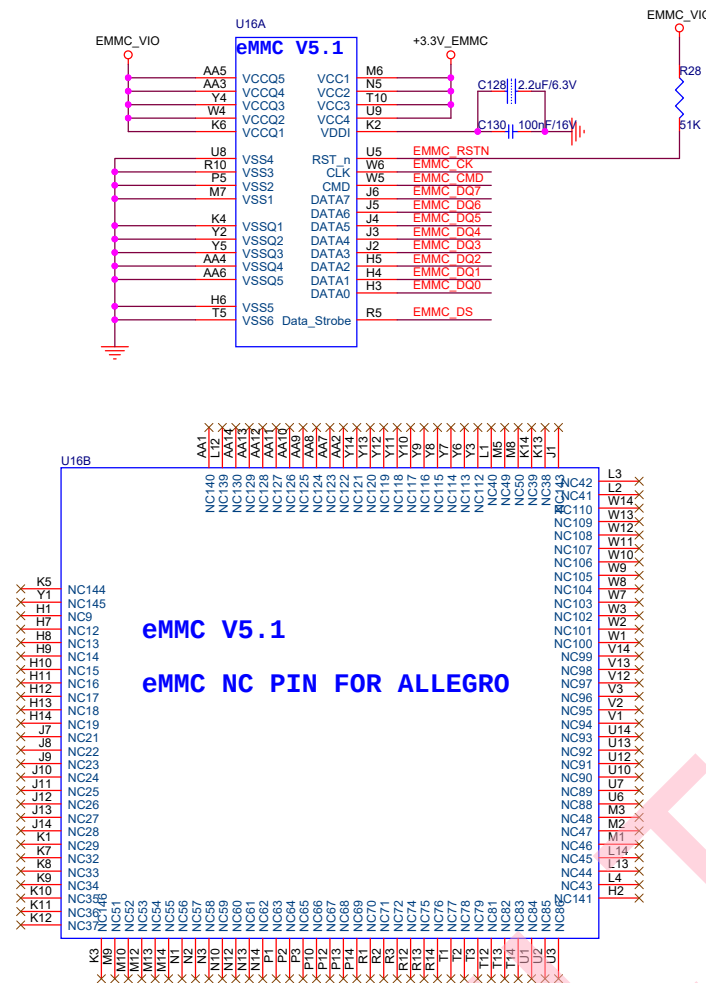
BackLight Controler



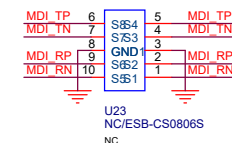
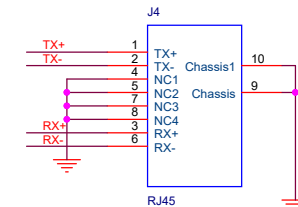
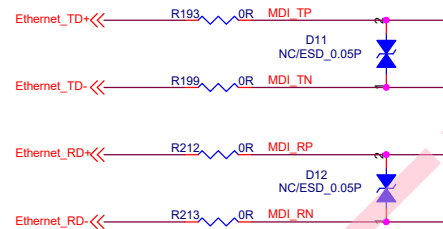
MARK & HOLE



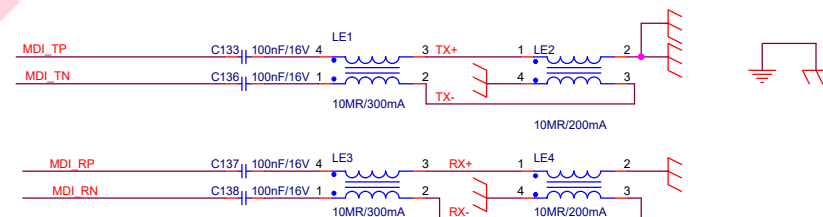
EMMC



Ethernet Connetor



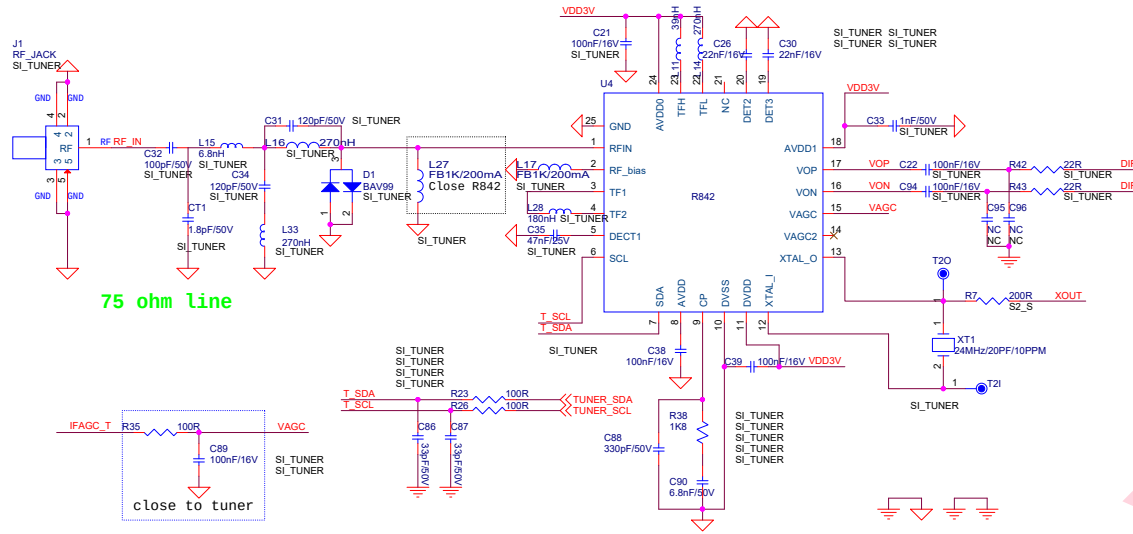
ENTHERNET 分立



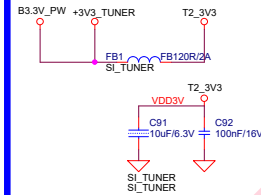
EMMC Power



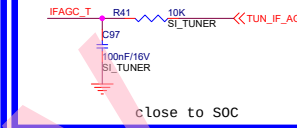
T/T2/C TUNER



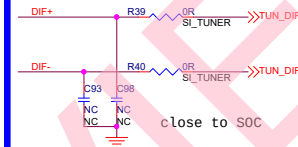
T2 Tuner Power



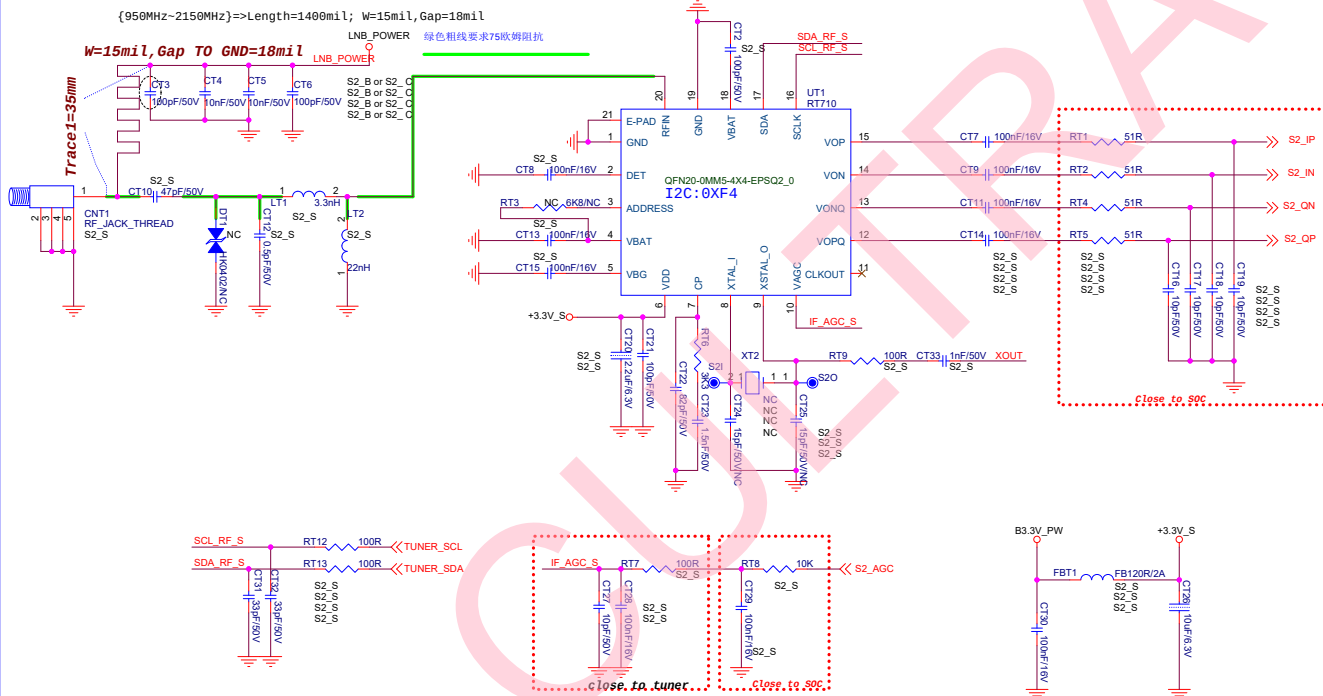
T2_AGC



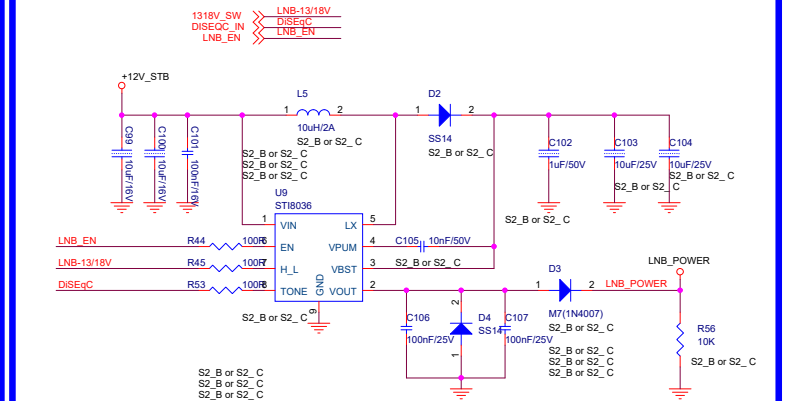
T2_IF



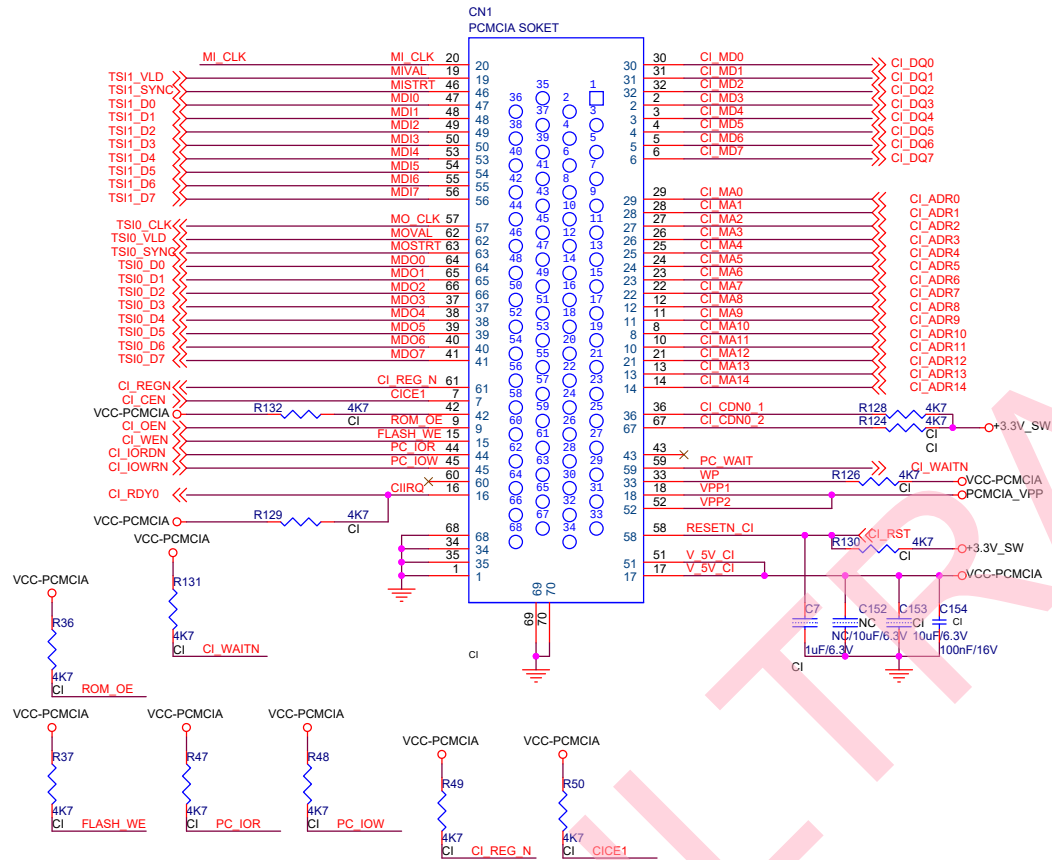
S2 TUNER



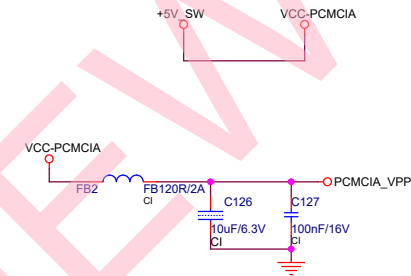
LNB POWER



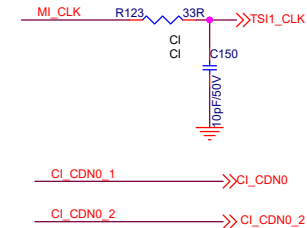
CI Socket



PCMCIA POWER



CLK



AMPLIFY

The diagram illustrates the PCB layout for the HAA3603 amplifier. The main layout shows the placement of components on the PCB, including capacitors (CA1-CA19), resistors (RA1-RA5), and the amplifier chip (UA1). The layout is divided into several sections: the main layout, a detailed view of the amplifier's internal structure, and a close-up of the main chip connection.

Main Layout:

- Inputs:** AMP_EN, AMP LIN, AMP_REF, AMP_POWER, AMP_RIN.
- Outputs:** AMP LOUT+, AMP LOUT-, AMP ROUT+, AMP ROUT-.
- Components:** CA1-CA19 (capacitors), RA1-RA5 (resistors), UA1 (HAA3603 amplifier chip).
- Pin Connections:** The chip pins are connected to the inputs, outputs, and power supply (VCC1, VCC2, VCC3, VCC4).

Detailed View:

- Inputs:** AMP_EN, AMP LIN, AMP_REF, AMP_POWER, AMP_RIN.
- Outputs:** AMP LOUT+, AMP LOUT-, AMP ROUT+, AMP ROUT-.
- Components:** CA1-CA19 (capacitors), RA1-RA5 (resistors), UA1 (HAA3603 amplifier chip).
- Pin Connections:** The chip pins are connected to the inputs, outputs, and power supply (VCC1, VCC2, VCC3, VCC4).

Close to Main Chip:

- Inputs:** AMP_EN, AMP LIN, AMP_REF, AMP_POWER, AMP_RIN.
- Outputs:** AMP LOUT+, AMP LOUT-, AMP ROUT+, AMP ROUT-.
- Components:** CA1-CA19 (capacitors), RA1-RA5 (resistors), UA1 (HAA3603 amplifier chip).
- Pin Connections:** The chip pins are connected to the inputs, outputs, and power supply (VCC1, VCC2, VCC3, VCC4).

Headphone OP

The diagram illustrates a Headphone OP circuit using the APA2172AOI-TRG (UA2) op-amp. The circuit includes input stages for AMP_RIN, AMP_REF, and AMP_LIN, and output stages for EAR_ROUT and EAR_LOUT. It also shows power supply connections for +12V_STB and +3.3V_SW, and various passive components like resistors (RA12-RA20) and capacitors (CA26-CA36).

MUTE

AMP_MUTE

RA10 4K7 AMP_EN

RA11 4K7

AMP MUTE
0: MUTE
1: NORMAL

EARPHONE

The diagram shows an earphone jack (J7) with pins 1 (GND), 2 (Audio L), 3 (Audio R), 4, and 5. The Audio L and Audio R signals are connected to the EAR LOUT and EAR DET pins of a CA31CA38 component, respectively. The CA31CA38 is also connected to a +3.3V_SW supply through a 4K7 resistor (R11) and a 47K resistor (RA23). The output of the CA31CA38 is connected to a 1K resistor (RA26) and a 4K7 resistor (R84). The output of the 4K7 resistor (R84) is connected to the IDENT_HP pin. The CA31CA38 is also connected to a 22nF/16V capacitor (CA3TCA38) and a 22nF/16V capacitor (CA3TCA38).

Earphone Detect;
H: Insert Earphone;
L: Pull Out Earphone;